REMARKS

This amendment is responsive to the non-Final Office Action of April 3, 2009. Reconsideration and allowance of claims 2-13 and 15-22 are requested.

The Office Action

Claims 1-10, 11, and 12-19 stand rejected under the doctrine of obviousness-type double-patenting relative to claims 1-10, 1, and 12-19 of the applicant's later filed US Application Serial No. 10/597,246.

Claims 1-10, 11, and 12-19 stand rejected under 35 U.S.C. § 101 for double-patenting over claims 1-10, 1, and 12-19 of copending US Application Serial No. 10/597,246.

Claim 20 stands rejected on unspecified grounds as being dependent on a claim rejected based on double-patenting, but is not itself rejected under double-patenting.

Claims 1, 2, 13, 14, and 16 stand rejected under 35 U.S.C. § 102 over Kozlowski (US 6,538,245).

Claims 10 and 19 stand rejected under 35 U.S.C. § 103 over Kozlowski in view of Kitamura (US 6,988,131).

Claims 3-9, 11, 12, 15, 17, 18, and 20 were indicated as containing allowable subject matter.

35 U.S.C. § 101 Double-Patenting

Claim 1 of US Application Serial No. 10/597,246 claims:

> and wherein each pixel further comprises a third transistor (49), the gate of the third transistor being connected to one terminal of the light sensor element (12) and the source of the third transistor (49) being connected to the gate of the first transistor (40).

This same limitation is incorporated in dependent claims 2-13 of US Application Serial No. 10/597,246. None of the claims of the present application specifically claim the transistor (49).

Independent claim 14 and claims 15-19 by virtue of their dependence on claim 14 of US Application Serial No. 10/597,246 call for:

> providing the sensor voltage (Vin) to an in-pixel voltage amplifier through a source-follower buffer transistor...

None of the claims of the present application claim this step.

Because the claims of the present application are not identical to the claims of US Application Serial No. 10/597,246, it is submitted that the 35 U.S.C. § 101 double-patenting rejection should be withdrawn.

Obviousness Double-Patenting

US Application Serial No. 10/597,246 differs from the present application at least in the inclusion of the source-follower transistor (49). It is submitted that this source-follower transistor (49) achieves numerous improvements. For example, the last paragraph of page 8 of US Application Serial No. 10/597,246 reads as follows:

> The additional source follower transistor 49 drives only the gate capacitance of the amplifier TFT 40 and is not disturbed in readout, so it can be made with small dimensions. This greatly reduces the size of the parasitic capacitance effective on the input storage capacitance 14. As the additional source follower transistor 49 is non-inverting and has no gain, the Miller effect is negligible. The larger Miller capacitance of the amplifier TFT 40 no longer effects the operation of the circuit as the buffer voltage-drives the amplifier input, so that the buffer replaces the lost charges.

Similarly, in discussing the problems with the prior art, page 2, third full paragraph of US Application Serial No. 10/597,246 states:

> However, a problem associated with the use of a voltage amplifier circuits arises as a result of the Miller effect. In particular, the input impedance of the voltage amplifier causes some of the input charge to be shared between an input storage capacitance and the parasitic gate-source capacitance of the drive transistor. The Miller effect tends to increase the apparent parasitic capacitance at this stage.

Similarly, page 3, first full paragraph of US Application Serial No. 10/597,246 states:

> In this arrangement [with a third transistor], each pixel provides gain through voltage amplification. This enables the sampling capacitor to be kept to a low size, so that the pixel circuitry occupies the smallest possible space, thereby enabling large aperture pixels to be formed. The amplifier arrangement of two series-connected transistors uses the requirement for equal source-drain currents to provide voltage amplification of the gate-source voltage signals. The third transistor acts as a buffer before signal amplification, and this overcomes the effect of charge sharing resulting from the parasitic capacitances of the first transistor of the voltage amplifier.

Thus, subsequent US Application Serial No. 10/597,246 recognizes a further improvement relative to the prior art, which further improvement is not disclosed or claimed in the present application. First, the further improvement flowing from the source-follower buffer transistor (49) sets forth a new and unexpected result (patentable improvement) over the claims of the present application and the prior art. Second, the Examiner has provided no evidence that the source-follower buffer transistor improvement of US Application Serial No. 10/597,246 is obvious over any of the claims of the present application.

Accordingly, it is submitted that the obviousness-type double-patenting rejection should be withdrawn.

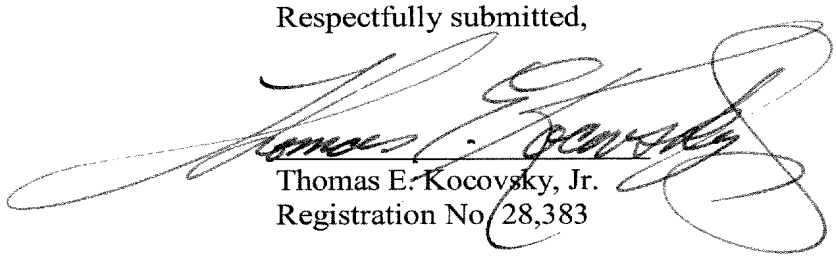
The Claims Distinguish Patentably Over the References of Record

Claims 3, 7, 11, 15, and 17 have been placed in independent form. Dependent claims 2, 4-6, 8-10, 13, 16, 19, and new claims 21-22 either are or have been amended to depend directly or indirectly from one of these claims. Because claims 3, 7, 11, 15, and 17 were indicated as containing allowable subject matter, it is submitted that all claims now distinguish patentably and unobviously over the references of record.

CONCLUSION

For the reasons set forth above, it is submitted that claims 2-13 and 15-22 distinguish patentably over the references of record. An early allowance of all claims is requested.

Respectfully submitted,



Thomas E. Kocovsky, Jr.
Registration No. 28,383

FAY SHARPE LLP
The Halle Building, 5th Floor
1228 Euclid Avenue
Cleveland, OH 44115-1843
Telephone: 216.363.9000 (main)
Telephone: 216.363.9122 (direct)
Facsimile: 216.363.9001
E-Mail: tkocovsky@faysharpe.com

Direct All Correspondence to:
Chris Ries, Reg. No. 45,799
US PHILIPS CORPORATION
P.O. Box 3001
Briarcliff Manor, NY 10510-8001
(914) 945-6000 (tel)
(914) 332-0615 (fax)